IN THE DRAWINGS

The attached sheet of drawings includes changes to Fig. 1. This sheet, which includes

Fig. 1, replaces the original sheet including Fig. 1.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Favorable reconsideration of this application as currently amended and in light of the following discussion is respectfully requested.

Claims 1, 3-9, and 11-17 are currently pending. The present Amendment amends Claims 1, 9, 11, 16, and 17; and cancels Claims 2 and 10 without prejudice or disclaimer. The changes to the claims are supported by the originally filed application. No new matter has been added.

In the outstanding Office Action, the drawings were objected to because of informalities; Claim 16 was objected to because of informalities; Claims 1-16 were rejected under 35 U.S.C. § 101 as directed to non-statutory subject matter; Claims 1, 6, 8, 9, 14, 16, and 17 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukuda et al. (U.S. Patent No. 6,099,574, herein "Fukuda") in view of Hirotaka (Japanese Patent Application No. 08-282456); Claims 5, 7, 13, and 15 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukuda and Hirotaka, further in view of Kenichi (Japanese Patent Application No. 03-247342); and Claims 2-4 and 10-12 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Fukuda and Hirotaka, further in view of Jachimowicz (U.S. Patent No. 5,821,911).

In response to the objection to the drawings, submitted herewith is a Letter Submitting Replacement Drawing Sheet(s) along with one Replacement Sheet for Fig. 1 in which a typographical error has been corrected. Specifically, reference "121" has been replaced by "112." Accordingly, the drawings are now believed to be compliant and no further objection on this basis is anticipated.

In response to the objection to Claim 16 because of informalities, Claim 16 is amended to correct the cited informalities. Specifically, "method" has been replaced with "program product" in the preamble of Claim 16. Accordingly, the grounds for the objection

are believed to have been overcome. Therefore, it is respectfully requested that the objection to Claim 16 be withdrawn.

Applicant noted typographical errors in the specification. Specifically, "?" was introduced in place of "θ" as a result of an incompatibility between the Japanese and original versions of Windows. The specification is amended to correct this error. It is respectfully submitted that the use of "θ" to represent an angle is well known in the art and that this correction does not introduce new matter.

Applicant respectfully requests reconsideration of the rejection of Claims 1-16 under 35 U.S.C. § 101 for the reasons discussed below.

The Office Action asserts at page 5 that "[t]he invention is not **useful** since the method and product of claims 1-16 does not recite a <u>result</u> that is useful in the technological art. This makes it difficult to determine Applicant's invention since it merely claims a manipulation of abstract ideas, which carrying out a simulation with simulation data." Applicant respectfully disagrees and submits that a simulation is not an idea nor is it abstract. For instance, architects make simulations of buildings so that they can test the building's architecture against a plane impact, for example, without having to actually test such an impact. Such an impact simulation may be represented as data in a computer, but is it in itself a result, and a very useful one. Likewise, Applicant's invention yields a simulation of a semiconductor device. The simulation itself is a result, and a useful one, as it allows the development of semiconductor devices. Now, in addition to this useful result, the simulation also ultimately leads to an actual simulation device. In the spirit of moving prosecution forward, Applicant amends independent Claims 1 and 9 to recite this second useful result. Specifically, amended independent Claims 1 and 9 now recite "simulation for designing *a semiconductor device*." It is respectfully submitted that the usefulness of a semiconductor device is beyond any question.

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The Office Action further asserts at page 5 that "the claims are not **tangible** since, for example, the results of carrying out the simulation with the simulation data are not given." Applicant respectfully disagrees and submits that a simulation is a result in itself and that it is a tangible result. When a plane impact on a building is simulated, for example, parameters of the plane and the buildings are known and the simulation runs according to the rules of physics. When the impact occurs, a model calculates whether the building is more or less affected, and all of this is saved on a computer, to be displayed or printed and viewed by users, and constitutes the simulation. The simulation is thus very tangible. For example, it can be given to someone on a compact disk, or can be e-mailed to a colleague who can examine it and use it in various ways. Applicant further notes that the other result of amended independent Claims 1 and 9, the "semiconductor device," is clearly tangible.

The Office Action further asserts at page 5 that "the claims are not **concrete** because results are not assured. For example, the out come of the simulation with simulation data is not definite. Because the result of the simulation with simulation data is not given." Again, a simulation is a result in itself, and the fact that many outcomes are possible does not preclude every outcome, albeit perhaps different, from being concrete as is the case here.

In addition, Applicant respectfully submits the following discussion to further establish that the claimed subject matter is statutory and, in particular, highlight the useful, tangible, and concrete nature of the claimed subject matter.

A simulation of manufacturing processes or electric characteristics of a semiconductor device is usually restricted by various conditions such as a computation time and a computer memory capacity. To comply with the restrictions, the simulation is carried out by setting a finite calculation area. To reduce computation time, the calculation area is usually narrowed. Setting a finite calculation area for a simulation is achieved by setting boundary conditions on the boundary of the finite calculation area. The boundary conditions can include an influence on the calculation

area from the outside of the calculation area. Usually, the influence on the calculation area from outside of the calculation area cannot be bypassed for accurate simulation. This influence of the boundary conditions is often overlooked by a design engineer, especially an inexperienced engineer, and the design engineer is frequently unaware of a deviation in a simulation result from a true result to be derived from the simulation on the calculation area. Furthermore, since there are many kinds of boundary conditions, it is difficult to choose proper boundary conditions for the simulation. If improper boundary conditions are set for the simulation, an unintended simulation results, which if passed unnoticed to design a semiconductor device, can lead to a failure of the semiconductor device.

To solve this problem, Applicant's invention displays the virtual images that appear outside the calculation area 130 due to the boundary conditions, as shown in FIG. 3B. The calculation area 130 of FIG. 3B corresponds to that of FIG. 3A. The calculation area 130 includes the real images of the wires A and B. The non-calculation area outside the calculation area 130 includes the virtual images that are formed according to the mirror boundary conditions. The mirror boundary conditions form a virtual wire A on the left side of the calculation area 130. On the left side of this virtual wire A, a virtual wire B is formed due to the real wire B. With these images, the user easily understands whether or not the capacitance value to be computed is an intended one. Here, the term "virtual image" is the image that is outside of the boundary 130 in Fig. 3B. The term "real image" is the image that is inside of the boundary 130 in Fig. 3B.

It is thus respectfully submitted, for example, that Fig. 3B shows a useful, tangible, and concrete result. In particular, Applicant respectfully submits that had the claimed subject matter been directed to "abstract ideas," a tangible and concrete graphic representation suitable for examination and use by a user could not be displayed as it is in Fig. 3B.

To emphasize even further the useful, tangible, and concrete nature of the claimed subject matter, the features of Claims 2 and 10 are incorporated into Claims 1 and 9,

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respectively. Features of embodiments of the invention display both virtual and real images to make a user recognize the influence from outside of the boundary before the process or device simulation.

Applicant respectfully requests reconsideration of the rejection of Claims 1, 6, 8, 9, 14, 16, and 17 under 35 U.S.C. § 103(a) for the reasons set forth below.

Amended independent Claim 1 is directed to a method of simulation for designing a semiconductor device with simulation data of the semiconductor device, including: (1) determining whether or not the simulation data includes boundary conditions set for a boundary of a calculation area set for the simulation; (2) computing the influence of the boundary conditions on the inside of the calculation area if the simulation data include the boundary conditions; (3) displaying the influence of the boundary conditions on the inside of the calculation area, the displaying operation including: if the simulation data includes the boundary conditions, generating virtual images outside the calculation area according to the boundary conditions; and displaying the virtual images, as well as real images included in the calculation area; (4) prompting to enter an instruction whether or not the boundary conditions are changed; and (5) if an instruction to make no change in the boundary conditions is entered, carrying out the simulation with the simulation data. Amended independent Claim 9 recites similar features, but is directed to a computer program product.

Fukuda discusses a method for carrying out process simulation to obtain the geometry of semiconductor devices as well as the distribution profiles of impurities and defects in those devices. The process simulation for semiconductor devices of Fukuda handles plural same impurities introduced in different processes as different impurities. Thus, by handling those same impurities as different impurities in the calculation, Fukuda makes it possible to obtain distribution profiles of impurities in semiconductor devices that are not affected by another same impurity introduced in another process, or a number of processes, during processing.

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The Office Action asserts that the displaying step of independent Claim 1 is disclosed in column 15, line 30, of Fukuda. However, this passage, which states that "[t]o carry out third simulation or the device simulation (step 302), necessary data of application voltage, current, and other electrical *boundary conditions* together with device structures and impurity distribution profiles obtained by process simulation (step 301) are supplied to the device simulator," merely mentions electrical boundary conditions supplied to the device simulator and does not teach or suggest "displaying the *influence* of the boundary conditions on the inside of the calculation area" and "if the simulation data includes the boundary conditions, *generating virtual images outside the calculation area according to the boundary conditions*; and *displaying the virtual images, as well as real images included in the calculation area*," as recited in amended independent Claim 1 (and similarly recited in amended independent Claims 9 and 17). Further, Applicant respectfully submits that these features are not taught or suggested by Hirotaka either.

Applicant further respectfully submits that the technique of Fukuda is mainly used during the process simulation. However, Applicant's invention, whereas not limited to this terminology in any way, is a so-called pre-simulation technique. That is, the user is made to recognize the boundary conditions before the simulation. Applicant's invention and Fukuda are thus fundamentally different for this additional reason.

The Office Action asserts that Hirotaka, which is directed to a simulation method for obtaining a high precision analysis in a narrow calculation region, discloses a calculation area. However, Hirotaka's method is used mainly during the process simulation, is not a pre-simulation technique, and does not teach of suggest the afore-mentioned features not taught by Fukuda.

Therefore, even if the combination of Fukuda and Hirotaka is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach or suggest "displaying the *influence* of the boundary conditions on

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the inside of the calculation area" and "if the simulation data includes the boundary

conditions, *generating virtual images outside the calculation area according to the*

boundary conditions; and *displaying the virtual images, as well as real images included in*

the calculation area," as recited in amended independent Claim 1 (and similarly recited in

amended independent Claims 9 and 17). Accordingly, Applicant respectfully traverses, and

requests reconsideration of, this rejection based on Fukuda and Hirotaka.[1]

Applicant respectfully requests reconsideration of the rejection of Claims 5, 7, 13, and

15 under 35 U.S.C. § 103(a) for the reasons set forth below.

Applicant respectfully submits that Kenichi does not teach or suggest the afore-

mentioned features of amended independent Claims 1, 9, and 17 not taught by Fukuda and

Hirotaka. Further, whereas the Office Action asserts that page 1, lines 6-12, of Kenichi discloses

an expanded calculation area and changeable calculation area, it is respectfully submitted that this

passage of Kenichi teaches updating the value only by computing the area by supplying a boundary

condition for a selected area if the selected area is smaller than the whole. Therefore, Kenichi does

not disclose *expanding* the calculation area. Furthermore, the technique of Kenichi is used mainly

during the process simulation and is not a pre-simulation technique.

Therefore, even if the combination of Fukuda, Hirotaka, and Kenichi is assumed to be

proper, the combination fails to teach every element of the claimed invention. Specifically,

the combination fails to teach or suggest at least "displaying the *influence* of the boundary

conditions on the inside of the calculation area" and "if the simulation data includes the

boundary conditions, *generating virtual images outside the calculation area according to*

the boundary conditions; and *displaying the virtual images, as well as real images included*

in the calculation area," as recited in amended independent Claim 1 (and similarly recited in

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[1] See MPEP 2142 stating, as one of the three "basic criteria [that] must be met" in order to establish a *prima facie* case of obviousness, that "the prior art reference (or references when combined) must teach or suggest all the claim limitations," (emphasis added). See also MPEP 2143.03: "All words in a claim must be considered in judging the patentability of that claim against the prior art."

amended independent Claim 9). Accordingly, Applicant respectfully traverses, and requests reconsideration of, this rejection based on Fukuda, Hirotaka, and Kenichi.

Applicant respectfully requests reconsideration of the rejection of Claims 2-4 and 10-12 under 35 U.S.C. § 103(a) for the reasons set forth below.

Applicant respectfully submits that Kenichi does not teach or suggest the afore-mentioned features of amended independent Claims 1, 9, and 17 not taught by Fukuda and Hirotaka. Further, whereas the Office Action asserts that Jachimowicz discloses virtual images and real images, Applicant notes that Jachimowicz only teaches a miniature color visual display including an optical system for producing, from the plurality of complete real images, a single virtual image in color and magnified so as to be viewable through the viewing aperture. Specifically, Jachimowicz states that "[T]he array of pixels on semiconductor chip 30 forms one-half of a complete real image and the light passing through optical system 33 forms one half of a greatly enlarged virtual image 35. To an eye represented at 34, virtual image 35 appears to be at a predetermined distance (determined by optical system 33) behind the entire structure. Virtual image 35, as seen from a viewing aperture (not shown) in the apparatus of FIG. 4 is illustrated in FIG. 5." It thus appears that Jachimowicz's virtual images and real images are combined optically. On the contrary, in Applicant's invention, the virtual images are not combined optically, correspond to the outside of the calculation area, and are generated according to the boundary conditions. It is respectfully submitted that Jachimowicz does not teach or suggest virtual images *outside the calculation area according to the boundary conditions*.

Therefore, even if the combination of Fukuda, Hirotaka, and Jachimowicz is assumed to be proper, the combination fails to teach every element of the claimed invention. Specifically, the combination fails to teach or suggest at least "displaying the *influence* of the boundary conditions on the inside of the calculation area" and "if the simulation data includes

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the boundary conditions, *generating virtual images outside the calculation area according to the boundary conditions*; and *displaying the virtual images, as well as real images included in the calculation area*," as recited in amended independent Claim 1 (and similarly recited in amended independent Claim 9). Accordingly, Applicant respectfully traverses, and requests reconsideration of, this rejection based on Fukuda, Hirotaka, and Jachimowicz.
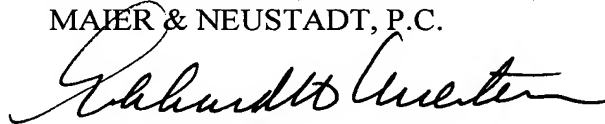
Finally, Applicant notes that the information disclosure statement filed on December 28, 2001, has not been initialed. To that effect, Applicant respectfully requests formal acknowledgment of the consideration of the information disclosure statement filed on December 28, 2001, with the next communication.

Consequently, in view of the present amendment, no further issues are believed to be outstanding in the present application, and the present application is believed to be in condition for formal Allowance. A Notice of Allowance for Claims 1, 3-9, and 11-17 is earnestly solicited.

Should the Examiner deem that any further action is necessary to place this application in even better form for allowance, the Examiner is encouraged to contact Applicant's undersigned representative at the below listed telephone number.

Respectfully submitted,

OBLON, SPIVAK, McCLELLAND,
MAIER & NEUSTADT, P.C.

Eckhard H. Kuesters
Attorney of Record
Registration No. 28,870

Customer Number

22850

Tel: (703) 413-3000
Fax: (703) 413 -2220
(OSMMN 06/04)
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